



# Intel® 82580EB/82580DB Gigabit Ethernet Controller

## Networking Division (ND)

### FEATURES

<p><b>External Interfaces Provided:</b></p> <ul style="list-style-type: none"><li>• PCIe v2.0 (5Gbps and 2.5Gbps) x4/x2/x1; called PCIe in this document.</li><li>• MDI (Copper) standard IEEE 802.3 Ethernet interface for 1000BASE-T, 100BASE-TX, and 10BASE-T applications (802.3, 802.3u, and 802.3ab)</li><li>• Serializer-Deserializer (SERDES) to support 1000Base-SX/LX (optical fiber)</li><li>• Serializer-Deserializer (SERDES) to support 1000BASE-KX and 1000BASE-BX for Gigabit backplane applications</li><li>• SGMII interface for SFP/external PHY connections</li><li>• NC-SI or SMBus for Manageability connection to MC</li><li>• IEEE 1149.6 JTAG</li></ul> <p><b>Performance Enhancements:</b></p> <ul style="list-style-type: none"><li>• Intel® I/O Acceleration Technology v3.0 supported:</li><li>• Stateless offloads (Header split, RSS)</li><li>• Direct Cache Access</li><li>• PCIe v2.1 TLP Processing Hints (TPH)</li><li>• UDP, TCP and IP Checksum offload</li><li>• UDP and TCP Transmit Segmentation Offload (TSO)</li><li>• SCTP receive and transmit checksum offload</li></ul> <p><b>Virtualization Ready:</b></p> <ul style="list-style-type: none"><li>• Enhanced VMDq1 support:</li><li>• Queues per port: 8 TX and 8 RX queues</li><li>• Support of up to 8 VMs per port (1 queue allocated to each VM)</li></ul>	<p><b>iSCSI*, PXE* and UEFI* Preboot Support</b></p> <ul style="list-style-type: none"><li>• iSCSI - SerDes, Fiber and Copper in Windows/Linux. SGMII is not currently supported.</li><li>• PXE - SerDes, Fiber, Copper, SGMII in Windows /Linux.</li><li>• UEFI - SerDes, Fiber, Copper, SGMII in Windows/Linux.</li></ul> <p><b>Power Saving Features:</b></p> <ul style="list-style-type: none"><li>• Advanced Configuration and Power Interface (ACPI) power management states and wake-up capability</li><li>• Advanced Power Management (APM) wake-up functionality</li><li>• Low power link-disconnect state</li><li>• PCIe v2.1 LTR (Latency Tolerance Reporting)</li><li>• DMA Coalescing for improved system power management</li></ul> <p><b>IEEE802.1AS - Timing and Synchronization:</b></p> <ul style="list-style-type: none"><li>• IEEE 1588 Precision Time Protocol support</li><li>• Per-packet timestamp</li></ul> <p><b>Total Cost Of Ownership (TCO):</b></p> <ul style="list-style-type: none"><li>• IPMI MC pass-thru; multi-drop NC-SI</li></ul> <p><b>Additional Product Details:</b></p> <ul style="list-style-type: none"><li>• 17x17 PBGA package</li><li>• Estimated power: 2.8W (max) in dual port mode and 4.2W (max) in quad port mode</li><li>• Full data path Parity or ECC protection</li></ul>
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## Revisions

Rev	Date	Notes
0.30	Dec 2008	Initial public release of early materials.
0.31	Jan 2009	<p><a href="#">Chapter 2.0</a>. Signals connected to the E14, F14, N12, R1, R2 and T1 corrected according to the latest ballout.</p> <p><a href="#">Section 11.4</a>. Updated power consumption estimates.</p> <p><a href="#">Table 11-21</a>. Corrected packaging information in the table. Now listed consistently as 17x17 PBGA package.</p>
0.5	2 April 2009	Updated EAS source used as base.
1.0	12 June 2009	Updated design information chapter added; supports Samples.
1.1	1 Oct 2009	Editorial Changes.
1.2	23 Oct 2009	<p><a href="#">Chapter 12.0, Design Guidelines</a> - 1.9V is no longer needed at the center tap. Language expressing that requirement has been removed.</p> <p><a href="#">Figure 11-1</a> and <a href="#">Table 11-3</a> updated to correct errors.</p>
1.3	5 Jan 2010	<ul style="list-style-type: none"> <li>• New EAS core added to Datasheet text.</li> <li>• Datasheet title updated to reflect dual and quad core capabilities.</li> <li>• Datasheet title changed to cover 'Dual' added.</li> <li>• <a href="#">Section 1.0, Introduction</a> language updated to indicate dual core support.</li> <li>• <a href="#">Table 2-7, SERDES/SGMII Pins</a> updated; now includes dual port exclusions. See asterisks.</li> <li>• <a href="#">Table 2-8, SFP Pins</a> updated; now includes dual port exclusions. See asterisks.</li> <li>• <a href="#">Table 2-9, LED Output Pins</a> updated; now includes dual port exclusions. See asterisks.</li> <li>• <a href="#">Table 2-10, Analog Pins</a> updated; now includes dual port exclusions. See asterisks.</li> <li>• <a href="#">Table 2-11, Testability Pins</a> updated; now includes dual port exclusions. See asterisks.</li> <li>• <a href="#">Table 2-15, Pin List in Alphabetical Order</a> updated; now summarizes all dual port exclusions. See asterisks.</li> <li>• <a href="#">Table 4-4, PCI Functions Mapping (Legacy Mode)</a> updated; information expanded.</li> <li>• <a href="#">Table 6-1, EEPROM Top Level Partitioning</a> updated; now includes dual port exclusions. See asterisks.</li> </ul>
2.0	15 Jan 2010	<ul style="list-style-type: none"> <li>• <a href="#">Section 7.8.2.4, Size Filtering</a> added.</li> <li>• <a href="#">Figure 12-4, Recommended Crystal Placement and Layout</a> on page 697 updated.</li> <li>• <a href="#">Chapter 13.0, Thermal Management</a> - Thermal management chapter added.</li> </ul>
2.1	15 Jan 2010	<ul style="list-style-type: none"> <li>• Test data updated.</li> </ul>
2.2	26 Feb 2010	<ul style="list-style-type: none"> <li>• <a href="#">Figure 12-5, Oscillator Solution</a> on page 698 updated.</li> <li>• <a href="#">Table 12-3, Oscillator Manufacturers and Part Numbers</a> updated.</li> <li>• Confidential stamp removed from document for posting on Developer.</li> </ul>
2.3	5 Mar 2010	<ul style="list-style-type: none"> <li>• In <a href="#">Section 13.4.4, Package Thermal Characteristics</a> ; <a href="#">Table 13-3</a> and <a href="#">Table 13-3</a> have been provided with updated data.</li> <li>• <a href="#">Appendix C., Changes from the 82576</a>; this appendix was added to the Datasheet.</li> </ul>



Rev	Date		Notes
2.4	29 Mar 2010		<ul style="list-style-type: none"> <li>In <a href="#">Section 6.2.5, Device ID (LAN Base Address + Offset 0x0D)</a>, the device ID was indicated as TBD because of a poorly set build variable. That has been corrected (Device ID = 1509).</li> <li>In <a href="#">Section 10.3.2.1.2, Request Status Command</a>, the descriptive paragraph has been updated for clarity.</li> <li>In <a href="#">Section 11.7.1, Mechanical</a>; ball, solder, and pad information has been added to the section.</li> </ul>
2.41	25 Jun 2010		<p>New sections:</p> <ul style="list-style-type: none"> <li><a href="#">Section 10.3.2.4, Filtering Over SMBus</a></li> <li><a href="#">Section 10.3.2.4.5, SMBus Troubleshooting</a></li> </ul> <p>Updated:</p> <ul style="list-style-type: none"> <li><a href="#">Section 7.2.5.3, SCTP CRC Offloading</a> updated. Note added: "Software must initialize the SCTP CRC field to zero (0x00000000) prior to requesting a CRC calculation offload."</li> <li><a href="#">Table 11-14, I<sup>2</sup>C Timing Parameters</a> updated. See T<sub>HD:DAT</sub>.</li> </ul>
2.42	7 Jul 2010		<p>The PCIe PHY Auto Configuration Pointer is not supported. The discussion of this capability has been removed from the datasheet.</p> <p>Two EEPROM registers exposed:</p> <ul style="list-style-type: none"> <li><a href="#">Section 6.2.14, PCIe Init Configuration 1 (Word 0x18)</a></li> <li><a href="#">Section 6.2.15, PCIe Init Configuration 2 Word (Word 0x19)</a></li> <li><a href="#">Section 6.2.16, PCIe Init Configuration 3 Word (Word 0x1A)</a></li> </ul>
2.43	20 Aug 2010		<p>Updated:</p> <ul style="list-style-type: none"> <li><a href="#">Table 2-13, Pull-Up Resistors</a>. For NCSI_CRD_DV change Note 2 to Note 1. For NCSI_TXD[1:0] changed PD to PU.</li> <li><a href="#">Section 6.11.5, PBA Number Module (Word 0x08, 0x09)</a>. This field has been updated. Its format has been changed.</li> <li><a href="#">Section 11.3.1, Power Supply Specification</a>. Value for Max Decoupling Capacitance changed to N/A..</li> <li><a href="#">Section 11.6.6, Oscillator Support</a>. Information on this topic is now in <a href="#">Section 12.5</a>.</li> </ul>
2.44	9/16/2010		<p>Updated:</p> <ul style="list-style-type: none"> <li><a href="#">Section 6.11.5, PBA Number Module (Word 0x08, 0x09)</a>. Language updated to address questions about final format.</li> </ul>
2.45	10/13/2010		<p>In the 2.44 build, the link to the Appendix did not appear in the PDF. This build fixes the issue. Also updated legal section.</p>



Rev	Date		Notes
2.46	3/23/2011		<ul style="list-style-type: none"> <li>Updated document title to better reflect brand string.</li> <li>Table 3-9, Allocation of FC Credits. First row cell text changed. Changed to: "Sixteen credit units to support tail write at wire speed."</li> <li>Section 6.11.1, Compatibility (Word 0x03). Word description updated.</li> <li>Section 6.11.2, Port Identification LED blinking (Word 0x04). Word description updated.</li> <li>Section 6.11.6.1, Setup Options PCI Function 0 (Word 0x30). Bits 2:0 redefined.</li> <li>Section 7.2.2.3.9, PAYLEN (18). Note text updated.</li> <li>Section 8.12.16, Tx Descriptor Completion Write-Back Address Low - TDWBAL (0xE038 + 0x40*n [n=0...7]; R/W). 32:2 bit description updated.</li> <li>Section 8.22.4, Management Control Register - MANC (0x5820; RW). Bit expression (20:2019) a typo. Corrected to 20:19.</li> <li>Table 11-24, Discrete/Integrated Magnetics Specifications. Added table, section with complete information on magnetics.</li> <li>Section 12.4.1.6, Load Capacitance. Text updated (formula corrected).</li> </ul>
2.47	4/6/2011		<ul style="list-style-type: none"> <li>Section 11.7.4, Package Schematics. Figure updated. Extraneous circle removed.</li> </ul>
2.48	5/10/2011		<ul style="list-style-type: none"> <li>Section 6.11.2, Port Identification LED blinking (Word 0x04). Text in section updated to better describe behavior.</li> </ul>
2.49	8/22/2011		<ul style="list-style-type: none"> <li>Table 6-2; 0x23 link fixed.</li> <li>Section 8.5.5, Flow Control Receive Threshold Low - FCRTL0 (0x2160; R/W). Phrase changed: "1b (at least 16 bytes)" to "3b (at least 48 bytes)".</li> <li>Table 10-2: In third row, existing text the existing text: "Supports counter 2 and also supports the following counters only when the OS is down: 1, 6, 7" has been changed to: "Supports the following counters: 1, 2, 6, 7."</li> <li>Section 13.2, Note added at end of section: "For the 82580EB/DB, Tjmax is calculated at 123 °C."</li> </ul>



Rev	Date		Notes
2.50	10/20/2011		<ul style="list-style-type: none"> <li>• More Preboot data added to feature summary on page 1.</li> <li>• <a href="#">Section 1.4.2, Network Interfaces</a>. Note added. States that old MDI flip-chip option not supported.</li> <li>• <a href="#">Section 1.4.3, EEPROM Interface</a>. Note on EEPROMless support added. States clearly that EEPROMless mode is not supported.</li> <li>• <a href="#">Section 1.4.5, SMBus Interface</a>. Statement added. Makes performance requirement clear: "For best performance, each 82580EB/DB should have its own dedicated SMBus link to the SMBus master device."</li> <li>• <a href="#">Section 1.6.12.2, Time SYNC (IEEE1588 and IEEE 802.1AS)</a>. Statement added. Clearly defines the limited nature of 1588 support.</li> <li>• <a href="#">Table 2-6, Miscellaneous Pins</a>. Note added to TSENSP; Note states limits of TSENSP/Z use. Refers to thermal chapter.</li> <li>• <a href="#">Table 2-10, Analog Pins</a>. Error corrected. RSVD_TX_TCLK clock speed indicated as 125 MHz instead of 1.25 MHz.</li> <li>• <a href="#">Section 2.5, Pin List (Alphabetical)</a>, <a href="#">Section 2.6, Ball-Out</a>. Note added. Makes clear statement about proper handling for 'unused pins'.</li> <li>• <a href="#">Section 6.2.15, PCIe Init Configuration 2 Word (Word 0x19)</a>. Note added to IO_Sup, bit14. The note defines 'disable I/O mode'.</li> <li>• <a href="#">Section 6.2.22, Functions Control (Word 0x21)</a>, bit 9 description; <a href="#">Section 9.4.11.2, 64-bit BARs Mode Mapping</a>, bit 3 description. Description has been changed. New text for both: "This bit should be set only on systems that do not generate prefetchable cycles."</li> <li>• <a href="#">Table 8-10, Usable FLASH Size and CSR Mapping Window Size</a>. Table added to Datasheet.</li> <li>• <a href="#">Section 11.3, Power Delivery</a>. Sentence added. Makes the following clear statement about power delivery: "The device requires the following power supplies: 3.3v, 1.8v, 1.0v. All 82580EB/DB power should be derived from AUX power."</li> </ul>
2.51	September 7, 2012		<ul style="list-style-type: none"> <li>• <a href="#">Section 2.1.4, NC-SI Interface Pins</a>. Notes added. They specify pull-ups/downs used when NC-SI is disconnected.</li> <li>• <a href="#">Section 5.5.5, Timing Requirements</a>, <a href="#">Section 5.5.6, Timing Guarantees</a>; both added to the datasheet.</li> <li>• <a href="#">Section 8.8.10, Interrupt Cause Set Register - ICS (0x1504; WO)</a>, <a href="#">Section 8.8.11, Interrupt Mask Set/Read Register - IMS (0x1508; R/W)</a>, <a href="#">Section 8.8.12, Interrupt Mask Clear Register - IMC (0x150C; WO)</a>; Time Sync Bit [19] added to the datasheet for all three registers.</li> <li>• <a href="#">Section 9.6.4.2, LTR Capabilities (0x1C4; RW)</a>. Description of Bits 15:13 and 31:29 corrected to RO.</li> </ul>
2.6	June 2014		<ul style="list-style-type: none"> <li>• Revised sections: 6.2.17 3.2.1.1.4 3.5.6.3.1 7.8.9 3.5.6.4 (new)</li> <li>• Revised tables: 2-15 7-6</li> </ul>
2.7	September 2015		<ul style="list-style-type: none"> <li>• Revised sections 6.11.7</li> <li>• Revised Table 11-22</li> </ul>



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